second inverter stage EI2 whose output is also coupled to the gate G of the switching transistor TC.

[0043] The first inverter stage EI1 comprises here, for example, a three-state voltage inverter **9** powered by the larger of the input VIN and output VOUT voltages and the ground GND. The structure of a voltage inverter **9** is known per se to the person skilled in the art. This inverter **9** receives at its first input a first control signal SC1 to invert at its output on the gate of the switch, and at its second input a second control signal SC2 to enable operation of the three-state voltage inverter **9**.

[0044] When the second control signal SC2 is in the low state, the first control signal SC1 is inverted on the gate G of the switching transistor TC. In the converse case, that is to say when the second control signal SC2 is in the high state, the voltage inverter **9** is in a high-impedance state.

[0045] It should be noted that the first inverter stage EI1 is not indispensable for the charge switch circuit **3** and that if the second control signal SC2 is in the low state, the input voltage VIN of the switch **3** is presumed be handled upstream in such a way as to limit a rapid variation that could lead to positive or negative inrush currents CE+, CE−.

[0046] When the first inverter stage EI1 is operating, the second inverter stage EI2, the first and second adjustment stages ER1 and ER2, and the comparator stage **7** are all configured to be deactivated.

[0047] The second inverter stage EI2 comprises here, for example, a so-called "starved" voltage inverter **10** having a limited current. This amplifier **10** is powered between the larger of the input VIN and output VOUT voltages and the ground GND through a reference current source SCR when the second control signal SC2 is in the high state.

[0048] The second inverter stage EI2 receives at its input the first control signal SC1 and delivers at its output the gate voltage VG of the switching transistor TC.

[0049] The reference current source SCR can be a simple current source, for example, comprising a current mirror generating a current proportional to the absolute temperature. This current source can, for example, also be used in the first and second adjustment stages ER1 and ER2, which will be detailed hereinafter.

[0050] It should be noted that the reference current source SCR is intended to limit the force of the voltage inverter **10** when the inverter **10** pulls the gate voltage VG of the switching transistor TC downwards in such a way as to allow the first or the second adjustment stage ER1 and ER2 to pull the gate voltage VG upwards.

[0051] The comparator stage **7** receives the input voltage VIN at its positive input and the output voltage VOUT at its negative input, and delivers the selection signal SS at its output.

[0052] When the input voltage VIN is greater than the output voltage VOUT, the selection signal SS is, for example, in the low state.

[0053] In the converse case, the input voltage VIN is less than the output voltage VOUT, and the selection signal SS is in the high state.

[0054] The control stage EC is intended to receive the second control signal SC2 and the selection signal SS, and configured to deliver respectively to the first and second adjustment stages ER1, ER2, a first activation signal SA1 and a second activation signal SA2 as a function of the control signal SC2 and selection signal SS. The control stage EC can, for example, be embodied with a conventional logic circuit.

[0055] The first activation signal SA1 is in the high state when the second control signal SC2 is in the high state and the selection signal SS is in the low state. In that case, the first adjustment stage ER1 is activated.

[0056] The second activation signal SA2 is in the high state when the second control signal SC2 is in the high state and the selection signal SS is in the high state. In that case, the second adjustment stage ER2 is activated.

[0057] Reference is now made to FIG. **3** to schematically illustrate an exemplary embodiment of the first adjustment stage ER1.

[0058] The first adjustment stage ER1 comprises a first detection capacitor CD1 coupled to the output voltage VOUT and configured to transform a positive variation of the output voltage VOUT into a variation of a first internal current Iint1. A first current mirror module MMC1 comprises here, for example, a first current mirror of nMOS type known per se and having a current transfer ratio equal to N. A first reference current module MCR1 is configured to generate a first reference current Iref1. A first voltage adjustment module MRT1 comprises a first transistor TC1 of the pMOS type whose gate is coupled to the output of the first reference current module MCR1 and to the output of the first current mirror module MMC1, and whose source is coupled to the larger of the input VIN and output VOUT voltages and whose drain is coupled to the gate of the switch **6**.

[0059] The first current mirror module MMC1 comprises a first current mirror nMOS transistor TNMC1 arranged diode-fashion whose drain is coupled to the battery voltage VBAT via a first auxiliary transistor TAP1 of the pMOS type.

[0060] At its gate, the transistor TAP1 receives the first activation signal SA1. When the first activation signal SA1 is in the low state, the transistor TAP1 is in its "on" state. The transistor TNMC1 is thus biased by the battery voltage VBAT. It should be noted that the reference SA1 illustrated in FIG. **3** is a signal complementary to the first activation signal SA1.

[0061] When the first activation signal SA1 is in the high state, the transistor TAP1 is in its "off" state. The positive variation of the voltage VOUT is transformed into the variation of the first internal current Iint1 via the first detection capacitor CD1.

[0062] The first current mirror module MMC1 is in operation by virtue of the biasing of the transistor TNMC1 via the transistor TAP1 when the first activation signal SA1 is in the low state.

[0063] This dynamic structure advantageously allows activation of the first adjustment stage ER1 only when the first activation signal SA1 is in the high state.

[0064] The first current mirror module MMC1 is configured to generate a first intermediate current N*Iint1 on the basis of the first internal current Iint1.

[0065] If the first intermediate current N*Iint1 becomes greater than the first reference current Iref1, the voltage of the gate of the first transistor TC1 decreases and the voltage of the gate VG of the switching transistor TC is therefore pulled upwards.